REMARKS/ARGUMENTS

Upon entry of this Amendment, which amends claims 1, 7, 13, and 15, and adds new claims 17 – 20, claims 1 – 20 will be pending. In the Office Action, claims 1 – 3 were rejected under 35 U.S.C. §102(e) as being anticipated by Wang, et al. (U.S. Publication No. 2005/0166038, hereinafter "Wang"); claims 4, 8, and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wang in view of Mirsky (U.S. Publication No. 2001/0029515); and claims 5 – 7 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wang in view of Abbott, et al. (U.S. Patent No. 6,601,158, hereinafter "Abbott"). Applicant respectfully requests reconsideration of the claims in view of the amendments above and remarks below.

Claims 1 – 6

Claim 1 was rejected under 35 U.S.C. §102(a) as being anticipated by Wang. Applicant submits that Wang does not disclose or suggest every element of claim 1, as amended. For example, Wang does not disclose or suggest a control signal for selectively causing the at least one register to hold a data value from the bus for one or more processor cycles at the input of the at least one functional unit, the data value being obtainable at the input at a start of a next processor cycle upon being needed.

The rejection stated that Wang discloses a register as register file 214 in Fig.2. As described in paragraph 78 on page 6, source operands are usually read from the register file. Thus, pipeline stages may be forced to wait one or more cycles before the results are written. Also, Wang discloses a bypass mechanism that allows a subsequent instruction waiting to get the result value without writing to the register file and then reading from the register file. Applicant submits that both processes disclosed by Wang do not disclose or suggest every element of claim 1, as amended.

Claim 1 discloses that a data value from the bus is held for one or more processor cycles. Also, the data value is held at the input of the at least one functional unit such that the data value is obtainable at a start of a next processor cycle upon being needed. Accordingly, the data value is stored but also accessible at the start of a next processor cycle upon being needed. In Wang, the bypass mechanism does not disclose or suggest storing a data value for one or more processor cycles. Thus, the bypass mechanism in Wang does not disclose or suggest every element of claim 1, as amended. Further, storing the result in a register file and then reading the result in a register file does not disclose or suggest every element of claim 1, as amended. Rather, claim 1 stores a data value for one or more processor cycles at the input

of the at least one functional unit. As disclosed in Wang in Fig. 2, the base register file is not at the input of the at least one functional unit. Also, when the data is needed from the register file, a fetch instruction is executed to fetch the data and then the data is available. Data also has to be written into the register file in the previous clock cycle. Accordingly, the embodiments of the present invention store the data value in a register at the input of a functional unit where that data value is obtainable at the input at a start of a next processor cycle upon being needed. This provides for whose the need for values to be obtained from memory or a register file.

Accordingly, Applicant respectfully requests withdrawal of the rejection of claim 1. Claims 2 – 6 and 17 depend from claim 1 and thus derive patentability at least therefrom. These claims also recite additional novel and nonobvious features. For example, claim 17 recites wherein the data value is obtained from the at least one register without performing an access command to memory. As described in Wang, a register file is used in which a fetch command is needed to retrieve the data value. Thus, Wang does not disclose or suggest that the data value can be accessed without performing the access command to memory. Although the bypass mechanism is disclosed, the bypass mechanism does not store the data value for one or more processor cycles.

Claims 7 – 12 and 18

Applicant submits that claims 7 – 12 and 18 should be allowable for at least a similar rationale as discussed with respect to claim 1.

Applicant respectfully submits that the present claims are in condition for allowance and an early Notice of Allowance is earnestly sought. The undersigned may be contacted at the telephone number below at the Examiner's convenience if it would help in the prosecution of this matter.

Respectfully submitted,

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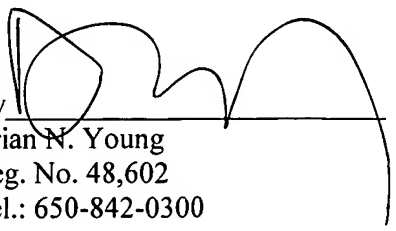

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